Studying Crosstalk Trends for Signal Integrity on Interconnects Using Finite Element Modeling

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Abstract

Introduction:
When talking of high-speed digital design, signal integrity is an inescapable issue and currently the focus of design engineers. Chips, Connectors and PCB Boards all have to stand the standard EMC Tests which include Noise, Timing, Crosstalk and Jitter among others. Many signal integrity problems are electromagnetic phenomena in nature and efficient field solvers such as the FEM based COMSOL Multiphysics® are useful for optimization and simulation of single level and multilevel interconnections. We consider Crosstalk which is the line to line coupling of energy through electric and magnetic fields. System level timings, propagation velocity, noise margins and signal integrity are greatly dependent on the characteristic impedance which is sensitive to crosstalk. Thus crosstalk trends need to be analyzed with respect to line to line spacing, substrate properties and other geometrical values, notwithstanding the constraints on these values placed by mechanical and routing restrictions.

Use of COMSOL:
COMSOL Multiphysics® was used to perform modeling and simulation of a microstrip structure consisting of single level interconnections. Using the ACDC Module, Electrostatics physics we extracted per unit length line parameters such as Inductance, Capacitance, and Characteristic impedance. Crosstalk was analyzed in worst case scenarios when one of the many interconnections was excited by truncated ramp, the standard excitatory signal in high speed digital design. This analysis was extended to multiple single level (layer) interconnections and multi-level interconnections. Finally a realistic case is considered for modeling the stack-up of standard 4-layer PCB (Figure 1). Using script tools, the model was optimized to minimize the worst-case crosstalks.

Results:
Since we are dealing with high speed 'digital' design, we analyzed the worst case crosstalk possibility. We varied the dielectric constants of substrate material, its thickness, the aspect ratio i.e. Interconnect separation/Width Ratio and heights of aggressors and victims and distance from ground plane. Results indicate that low-k dielectrics, thick substrates, large pitch ratio and maximum distance from ground plane are most suitable for minimizing crosstalk.
Refer to Figure 2, 3, 4.

Conclusion:

We start with the elementary 2 microstrip structure and extend the analysis to multi-level structure (stripline) and standard stack-up of 4-layer motherboard (4-layer pcb). Worst case analysis is done to determine the swing in characteristic impedance and velocity. Finally the chance of signal integrity being ruined is evaluated based on the possibility of crosstalk inducing false triggers. The safest geometry and medium properties are proposed.

Reference

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5.Stephen Hall, Garrett Hall,"High Speed Digital System Design: A handbook of interconnect theory and Design Practices", A Wiley Interscience Publication.

Figures used in the abstract

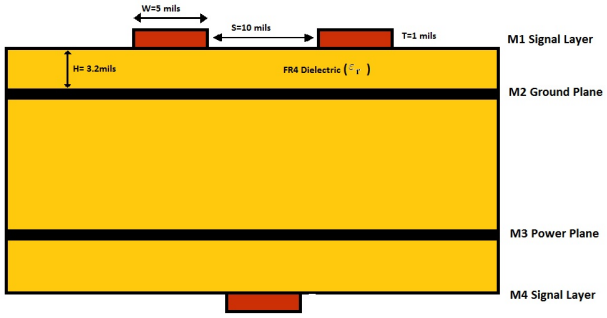

Figure 1: 4 layer stackup of PCB

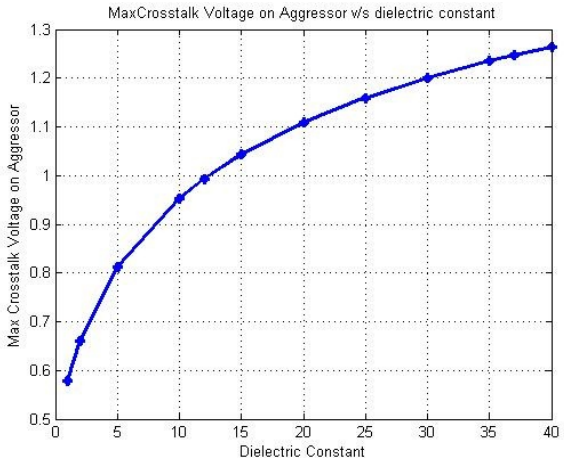

Figure 2: Crosstalk variation with Dielectric Constant

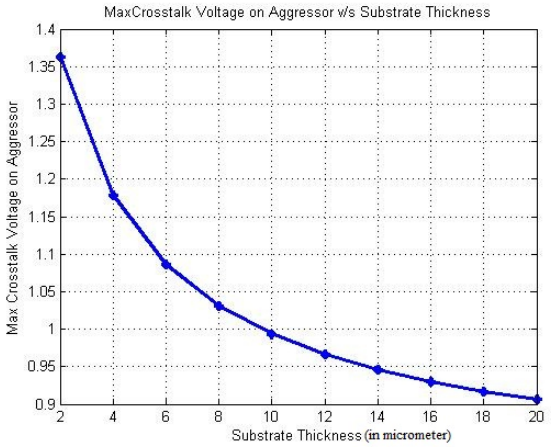

Figure 3: Crosstalk variation with Substrate Thickness

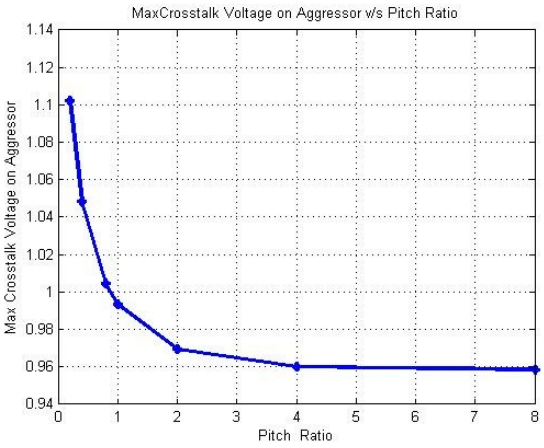

Figure 4: Crosstalk variation with Pitch Ratio