Fracture on Circuit Board Internal Layers Due to Thermal Stress on Soldered Pins

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Abstract

Introduction
Normally a failure on circuit boards is not easily discovered because even when a board looks perfectly well from the outside, doesn't mean that it is not damaged. With this simulation it is possible to examinate internal connections that are not visible. Temperature changes during the soldering process are modeled with COMSOL Multiphysics® to show the forces involved and determine the break points.

A 2D thermo-mechanical model (Figure 1) of a soldered pin is achieved in two simulation steps (as in the Model library examples [1]). Firstly, a connecting pin already attached to a fixed circuit board is placed in the via of a secondary circuit board, both are heated to a temperature according to the soldering process, then as a second step, the tin-solder is placed between the pin and secondary circuit board to finally let the system cool down.

Results
Stresses produced due to thermal deformation on the soldered area can be evaluated. A plot of the stress through the via will show how the internal layers and the connecting area are affected (Figure 2). Soldered pin connector interfaces used on expansion boards of electronic circuits, produce high stresses over the board connecting vias after the soldering process, which can produce the break of internal layer traces.

Conclusion
Analyzing the forces involved on the internal layers of the circuit board, demonstrates the possibility of rupture of the traces in connecting points. This simple 2D model of one connecting pin can be extended to a more complex model involving more pins.

Reference

[1] Structural Mechanics Module, Model Library, Thermal-Structure Interaction. COMSOL 4.3b.

Figures used in the abstract

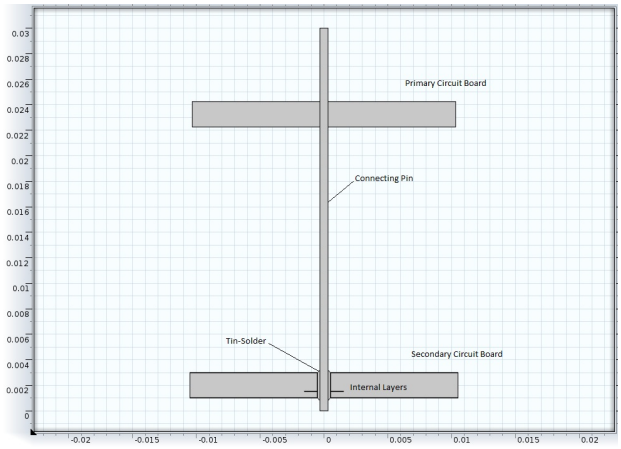

Figure 1

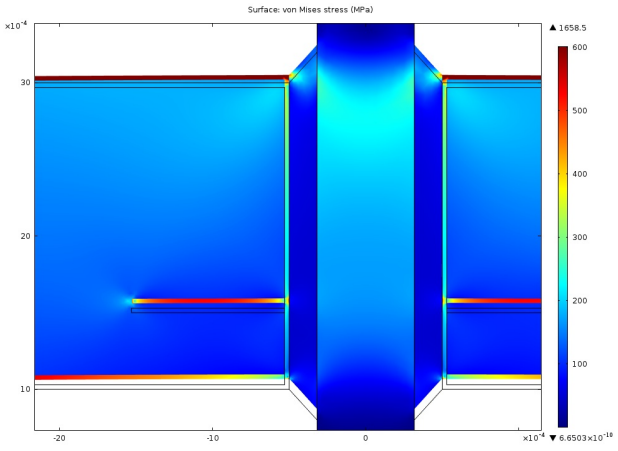

Figure 2