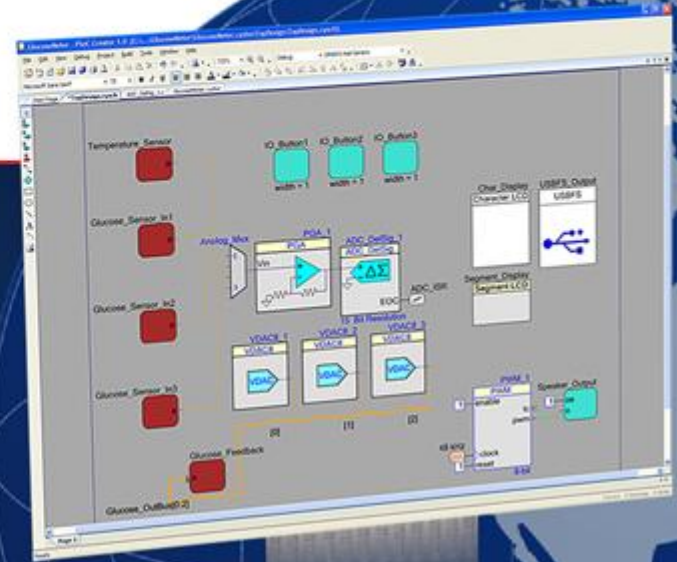


PROS AND CONS OF RUNNING COMSOL TOUCH- SENSOR SIMULATIONS ON AMAZON WEB SERVICES

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Cypress Semiconductor Corp.

- Founded in 1982 / Listed on the NASDAQ (CY)
- Broadest IP portfolio for touch-screens
- 4 billion mechanical buttons produced
- Over one billion touch solutions shipped
- Shipping to 9 of the top 10 mobile phone manufacturers
- Leading the way in touch for tablets – first to provide a high-performance single chip solution
- World's first market supplier of true multi-touch all-points touch-screen solution

Smartphones



ZTE
Nubia Z5



Huawei
Ascend
Mate



Fujitsu
Arrows V
F-04E



Samsung
Galaxy
Grand



Pantech
Vega R3

Tablets, Notebooks, E-Readers



Amazon
Kindle Fire
HD 8.9"

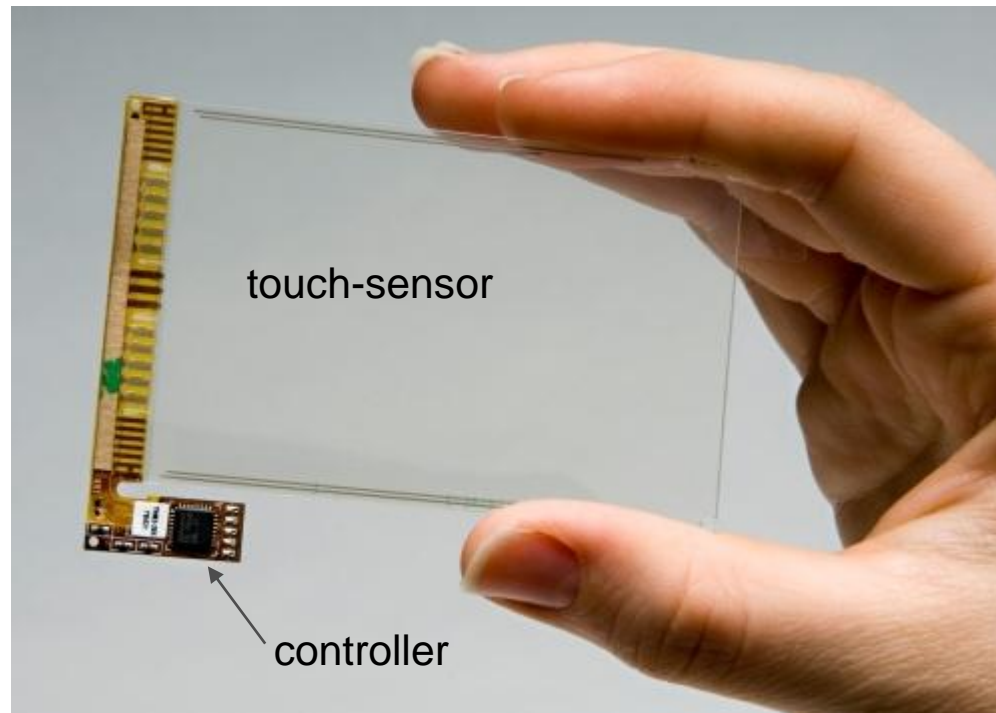


10.1" Fujitsu
Arrows Tab



6" Amazon
Kindle
Paperwhite

Capacitive Touch Screen

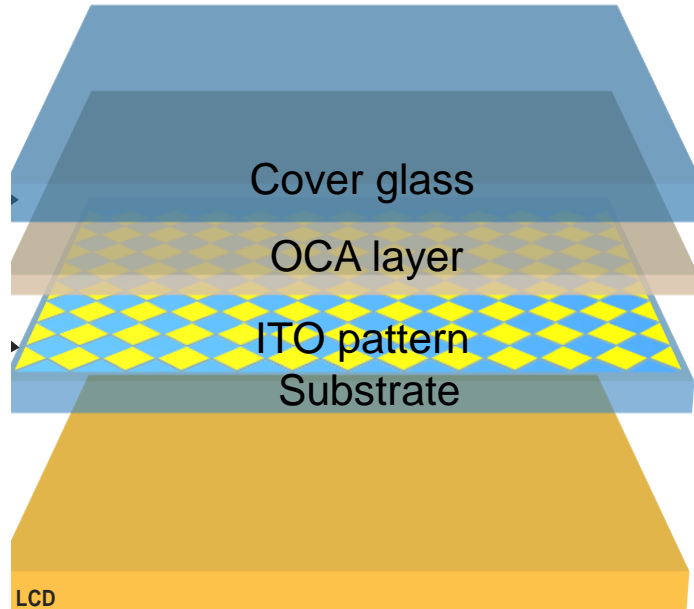


A basic touch-screen has three main components:

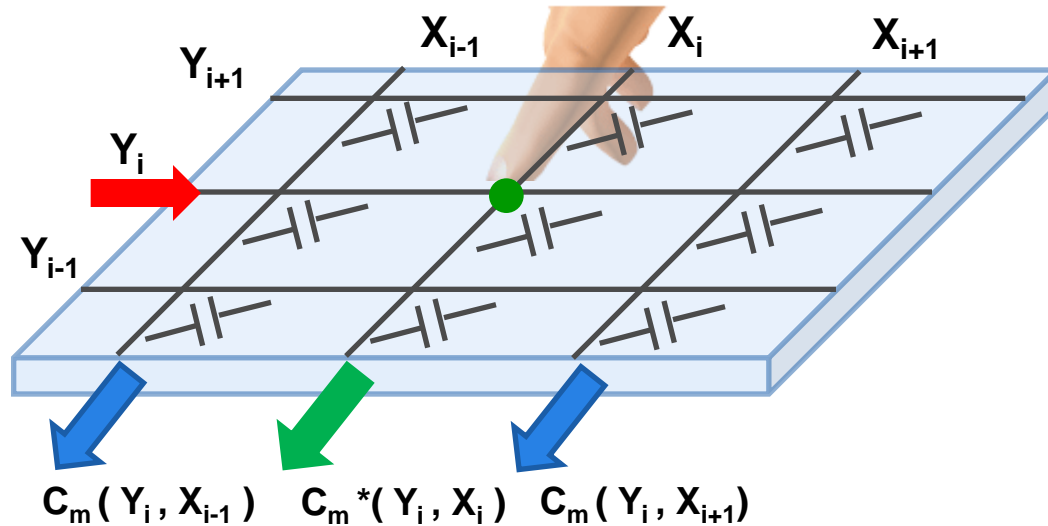
- Touch sensor
- Controller
- Software driver

Capacitive Touch Sensors

Sensor stack-up



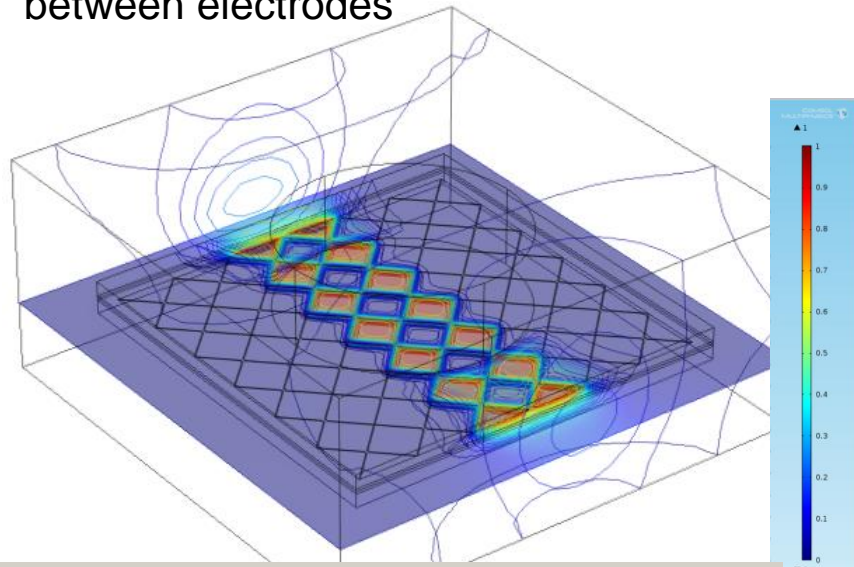
Finger touch detection



- Capacitive touch-sensors consist of one or two transparent conductive layers patterned onto substrates to produce horizontally (X_i) and vertically (Y_i) connected electrodes forming a grid structure.
- A touch object is sensed at the grid intersection. A finger touch on the screen surface distorts the electrostatic field. The touch is measurable as a change in coupling capacitance between horizontal and vertical electrodes.

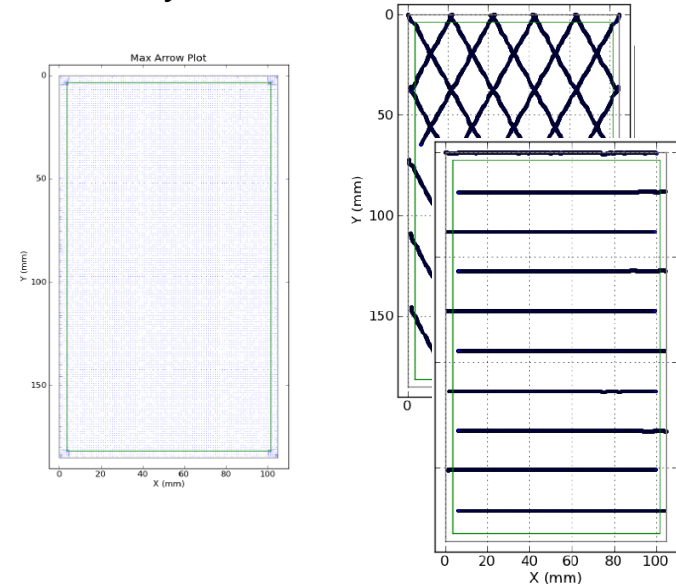
3D FEM simulations

OUTPUT: coupling capacitance between electrodes



System simulator

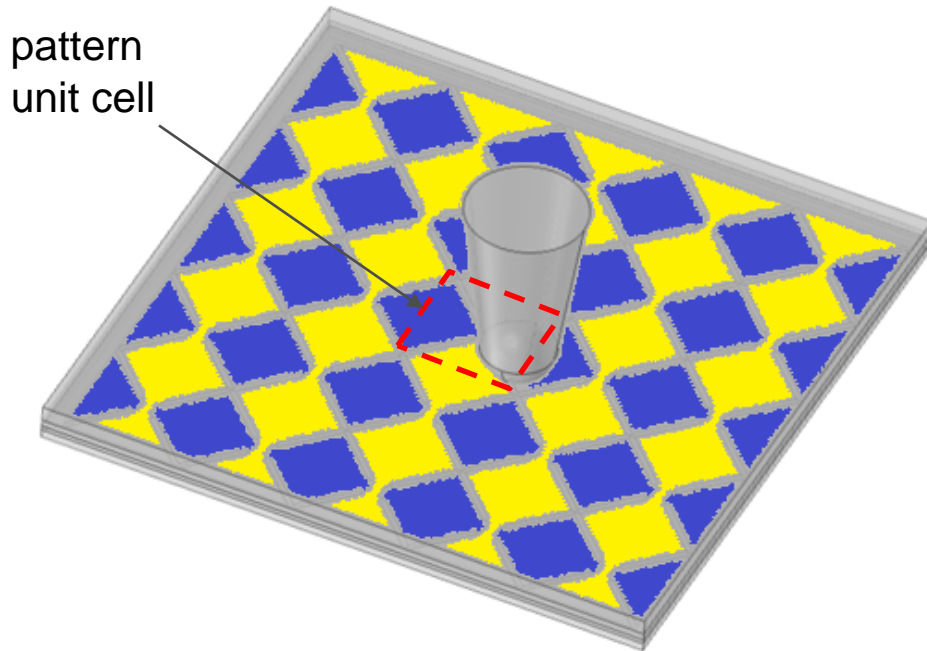
OUTPUT: sensor accuracy and linearity



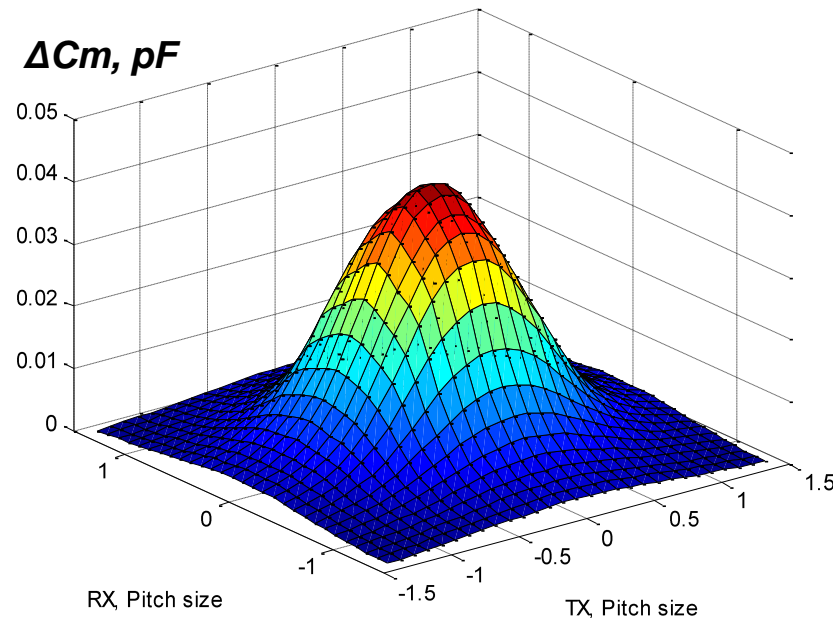
Multislice: Electric potential (V) Contour: Electric potential (V)

- Touch sensors have to track finger/stylus positions with high accuracy. System optimization is required to meet this goal.
- EM simulation data is an input to sensor accuracy/linearity simulations.
- System simulations require running numerous independent EM Comsol simulations with different finger/stylus positions.

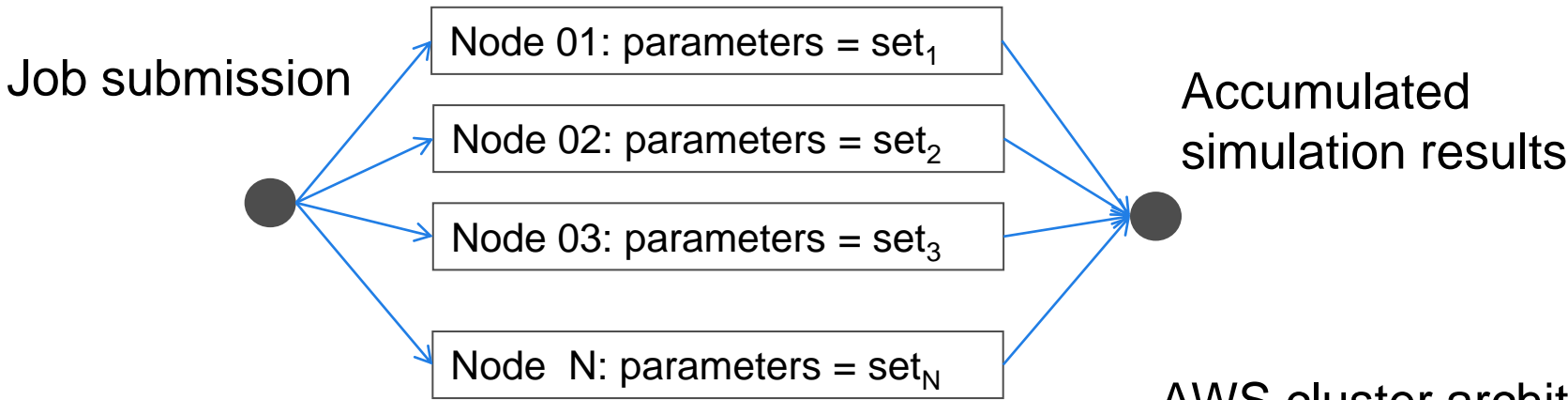
Comsol model set-up (5x5 array):



Stylus signal profile:

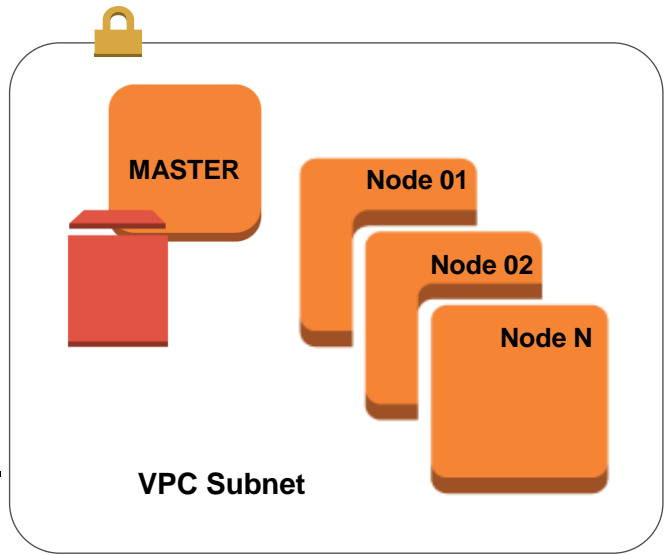


- The touch-sensor consists of a single-layer pattern embedded into a multi-layer stack-up. Diamond shaped electrodes are sequentially connected in rows & columns.
- The AC/DC Comsol model consists of a 5x5 array of identical unit cells.
- Mutual capacitance change (ΔC_m) due to stylus presence is detected at each electrode intersection. The right figure shows the signal profile for each stylus position with respect to the unit cell center.



- It is required to simulate at least 36 stylus positions within the unit cell to model sensor accuracy. Stylus coordinates & pattern geometry are defined as Comsol model parameters.
- Simulations can be submitted as an array of jobs that share the same executable and resource requirements, but have different input parameters.
- AWS cluster nodes were placed inside of the same VPC into a non-blocking 10 Gigabit Ethernet network.

AWS cluster architecture



Bash command: `bsub -J "Array[1-N]"`

Jobs Launched in Parallel on AWS Cluster

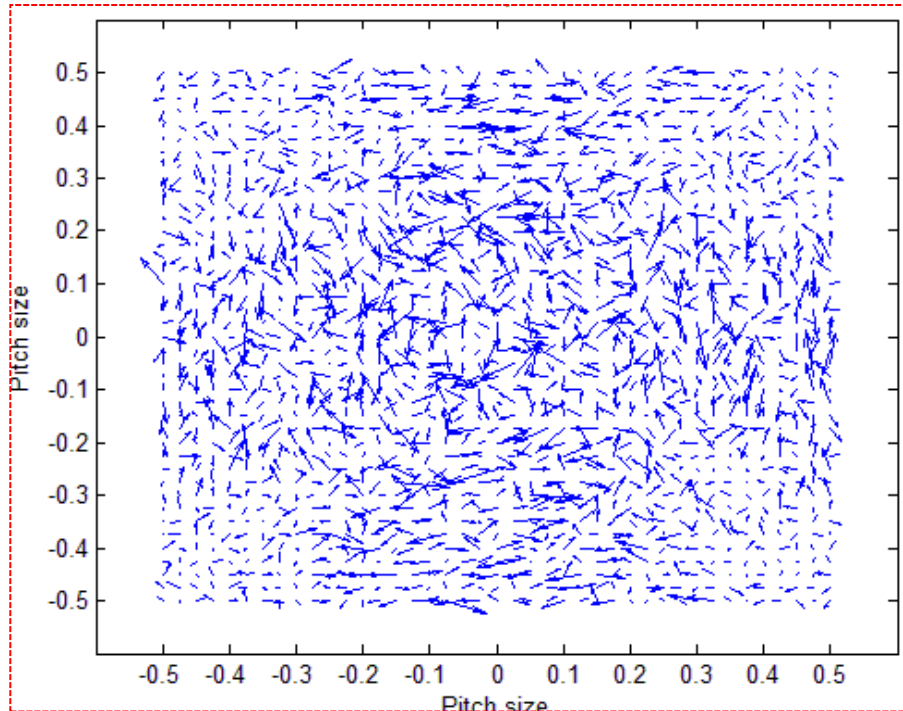


```
[comsol@ip-10-0-0-10 Run]$ bjobs
JOBID  USER  STAT  QUEUE  FROM_HOST  EXEC_HOST  JOB_NAME  SUBMIT_TIME
1      comsol  PEND  normal  ip-10-0-0-1  *bArray[1] Sep 24 21:34
1      comsol  PEND  normal  ip-10-0-0-1  *bArray[2] Sep 24 21:34
1      comsol  PEND  normal  ip-10-0-0-1  *bArray[3] Sep 24 21:34
1      comsol  PEND  normal  ip-10-0-0-1  [comsol@ip-10-0-0-10 Run]$ lshosts
HOST_NAME  type  model  cpuf  ncpu  maxmem  maxswp  server  RESOURCES
ip-10-0-1-2  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-9  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-3  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-2  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-1-1  linux  IntelI5 100.0  32  60922M  7161M  Yes  ()
ip-10-0-0-1  linux  IntelI5 100.0  4  14882M  -  Yes  (cs)
[comsol@ip-10-0-0-10 Run]$ bhosts
HOST_NAME  STATUS  JL/U  MAX  NJOBS  RUN  SSUSP  USUSP  RSV
ip-10-0-0-10  closed  -  4  0  0  0  0  0
ip-10-0-1-10  closed  -  32  32  32  0  0  0
ip-10-0-1-101  closed  -  32  32  32  0  0  0
ip-10-0-1-102  closed  -  32  32  32  0  0  0
ip-10-0-1-105  closed  -  32  32  32  0  0  0
ip-10-0-1-11  closed  -  32  32  32  0  0  0
ip-10-0-1-123  closed  -  32  32  32  0  0  0
ip-10-0-1-197  closed  -  32  32  32  0  0  0
ip-10-0-1-199  closed  -  32  32  32  0  0  0
ip-10-0-1-223  closed  -  32  32  32  0  0  0
ip-10-0-1-247  closed  -  32  32  32  0  0  0
ip-10-0-1-39  closed  -  32  32  32  0  0  0
ip-10-0-1-93  closed  -  32  32  32  0  0  0
1      comsol  PEND  normal  ip-10-0-0-1  *Array[35] Sep 24 21:34
1      comsol  PEND  normal  ip-10-0-0-1  *Array[36] Sep 24 21:34
```

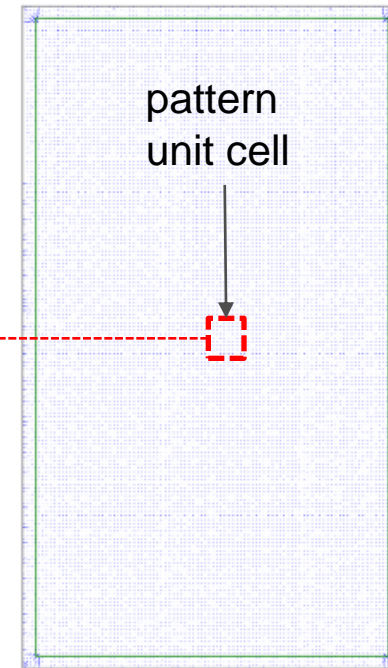
- 36 Comsol jobs are run in parallel from a master node.
- LSF scheduler deploys these jobs on available cluster nodes.

System Simulation Results: Sensor Accuracy

Arrow map within one pattern cell:

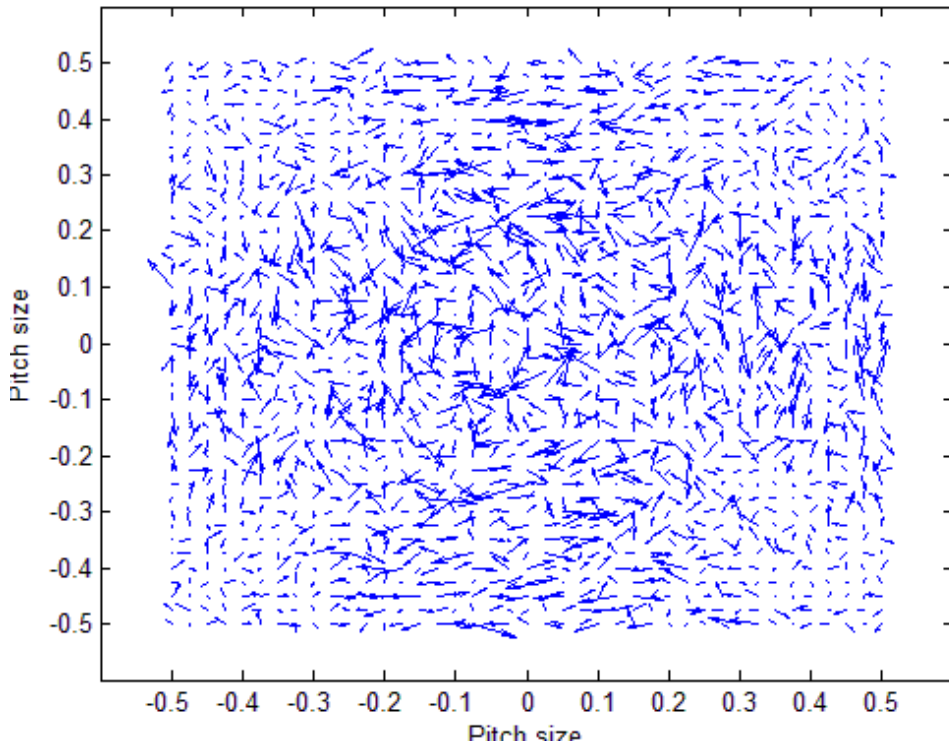


Touch-panel error map:

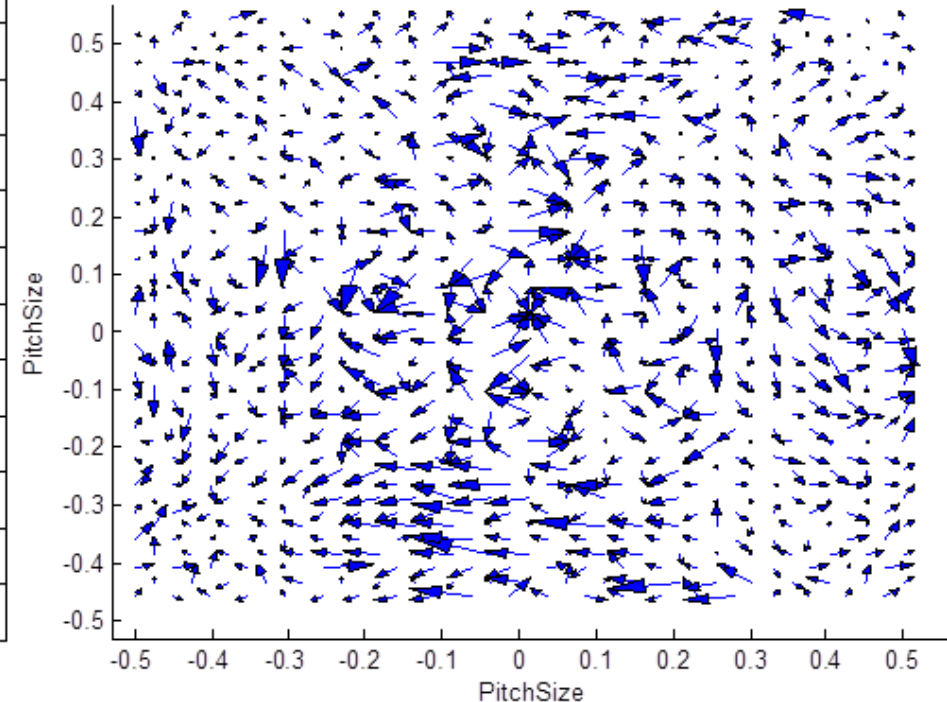


- The system simulator predicts the accuracy of the reported touch coordinates. The touch panel is an array of unit cell, so it is enough to determine the accuracy within one unit cell.
- The left graph shows an error map within the unit cell. The arrows represent the differences between the reported and real stylus positions.

Simulation data:



Characterization data:

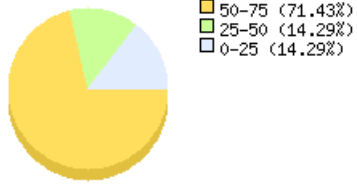


- To validate our methodology we compared simulation and characterization data.
- Both graphs show error maps of stylus position within one unit cell; arrow length represents an error in the reported stylus coordinates.

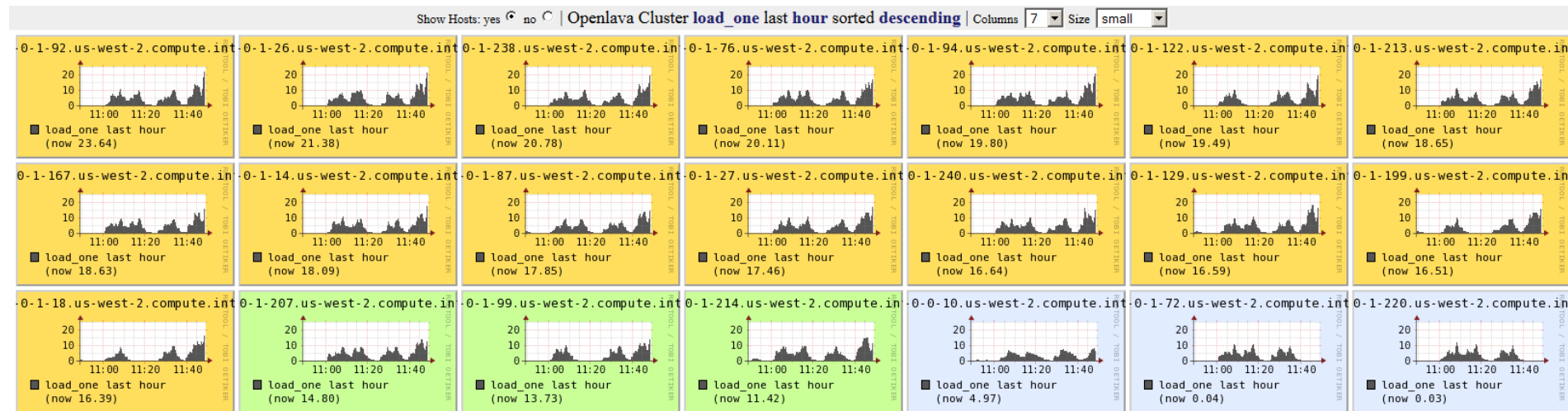
Usage of Cluster Computational Nodes



Cluster Load Percentages



AWS 20-node cluster load:



- An example AWS cloud cluster consists of twenty CC2 instances.
- Several Comsol jobs were run in parallel to test the cluster performance.
- The cluster performance was benchmarked with a performance on-premise DELL T5500 machine
- *CC2 instance: 60.5Gb RAM, 2 x Intel Xeon E5-2670 @ 2.6 GHz, eight-cores with hyperthreading*
Instances are placed into a non-blocking 10 Gigabit ethernet network.
- *DELL T5500: 48Gb RAM, 2 x Intel Xeon CPU X5680 @ 3.33 GHz, six-cores with hyperthreading*

Performance Benchmarking



Jobs	Nodes	Max jobs in parallel	Time, minutes	Node
36	20	20	~ 20 min	AWS-CC2
36	20	40	~ 10 min	AWS-CC2
36	1	1	> 4 hrs	T5500

- Several experiments were performed on the AWS cluster and the DELL T5500:
 - *36 Comsol jobs were run on a 20 node cluster. Only one job could be deployed on any cluster node at a time; new jobs were not allowed to run until the previous job finished. Total running jobs in parallel – 20.*
 - *36 Comsol jobs were run on the 20 node cluster. Two jobs could be deployed on any node at time; new jobs were not allowed to run until the previous jobs finished. Total running jobs in parallel – 36.*
 - *36 Comsol jobs were run in sequence on-premise DELL T5500 machine. Total running jobs in parallel – 1.*
- We observed 25X speed improvement by running experiment on the cluster

Pros and Cons of Running Comsol Simulations on AWS Cluster



■ PROS:

- *Horizontal (instance type) and vertical (cluster size) AWS resource scalability. Instances and number of cluster nodes can be optimized for each simulation task*
- *Comsol has no limit on the number of jobs running in parallel on cluster nodes*
- *Parallel computing significantly reduces simulation time*

■ CONS:

- *Comsol is a GUI oriented package, models require a lot of prep work to run on a Linux cluster using a shell script*
- *Cost of the cluster*

THANK YOU FOR ATTENTION, QUESTIONS.



Processor Specifications



Intel® Xeon® Processor E5-2670
(20M Cache, 2.60 GHz, 8.00 GT/s Intel® QPI)



Intel® Xeon® Processor X5680
(12M Cache, 3.33 GHz, 6.40 GT/s Intel® QPI)

SPECIFICATIONS

Essentials

Status	Launched
Launch Date	Q1'12
Processor Number	E5-2670
# of Cores	8
# of Threads	16
Clock Speed	2.6 GHz
Max Turbo Frequency	3.3 GHz
Cache	20 MB
Intel® QPI Speed	8 GT/s
# of QPI Links	2
Instruction Set	64-bit

SPECIFICATIONS

Essentials

Status	Launched
Launch Date	Q1'10
Processor Number	X5680
# of Cores	6
# of Threads	12
Clock Speed	3.33 GHz
Max Turbo Frequency	3.6 GHz
Intel® Smart Cache	12 MB
Intel® QPI Speed	6.4 GT/s
# of QPI Links	2
Instruction Set	64-bit