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MOSFET Channel Engineering and Scaling Study with Halo Implants Using COMSOL Multiphysics

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Abstract
As MOSFETs continue to be scaled to submicron dimensions, managing subthreshold current and threshold voltage becomes extremely important. This study focuses on 2-D MOSFETs built using COMSOL Multiphysics with silicon substrate and p-type halo implants introduced near the source and drain. Different mobility models, including the Arora, Lombardi surface, and Caughey-Thomas models were utilized to capture lattice scattering, surface scattering, and high-field effects. Electrical characteristics (I_d-V_g) were analyzed for MOSFETs of gate lengths of 397 nm, 280 nm, 196 nm, and 140 nm, following constant-field scaling trends. The results indicated a significant reduction in terminal current below the threshold voltage for halo-doped devices, effectively reducing leakage current. Additionally, an increase in threshold voltage was observed for the halo-doped MOSFETs.

Keywords: MOSFET, Constant Field Scaling, Halo Implants, COMSOL Multiphysics, Semiconductor

1. Introduction

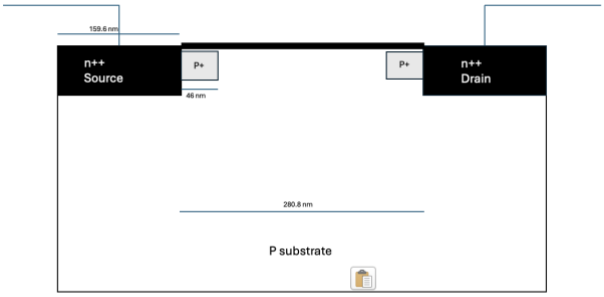
The continuous advancement and scaling of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFETs) have been an integral part of modern semiconductor technology. This has enabled higher performance, increased production and lower costs. However, as MOSFETs approach submicron and nanometer regimes, short channel-effects emerge as a major challenge. These effects include Drain-induced barrier lowering, impact ionization, velocity saturation and threshold voltage changes. A common approach to tackling these problems is to include a Lightly Doped Drain or LDD to the MOSFETs which can reduce impact ionization and hot-electron effects. [1]

Pocket implants like FIBMOS and Halo implants have also been used to reduce these short-channel effects. A study conducted by Hueting and his colleagues showed that Halo implants increase threshold voltage and reduce subthreshold voltage implying lower leakage. [2] Additionally, Saha and his co-workers used different halo architectures to show how threshold voltage variability is affected with different halo architectures.[3] This paper builds on the work of both and uses COMSOL Multiphysics to model and compare the effects of Constant Field Scaling on Halo-implanted MOSFETs compared to those of a conventional MOSFET. We analyze the different characteristics of Halo implants and how their threshold voltage and subthreshold voltage are affected in comparison to conventional MOSFETs. Simulation of these devices requires solving complex mathematical equations at various points in the device and is cumbersome. COMSOL Multiphysics is a simulation software that provides us with multiple modules with equations that help us do this for different conditions. We have included various Mobility Models such as the Arora, Lombardi surface, and Caughey-Thomas models to ensure that real-life effects such as lattice scattering, surface scattering, and high-field effects can be accounted for in our simulations.

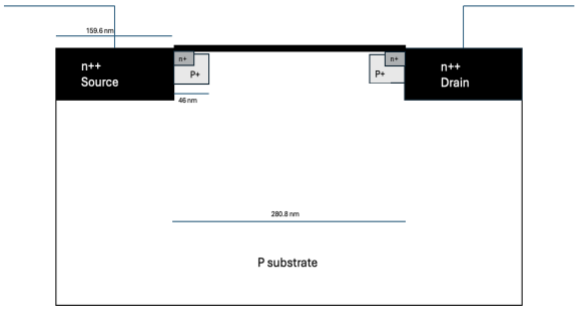
2. Theory/Experimental Set-up

2a) Device Structure

The general structure of a Halo-Implanted device is very similar to a conventional MOSFET but with the addition of two narrow p+ regions next to the source and the drain. We have used two different devices in this simulation where one is a conventional MOSFET with Halo implants and the second device also includes an LDD region to further reduce short-channel effects. Figure 1 shows the devices being simulated in this paper.



(a)



(b)

Figure 1. a) Schematic diagram of the structure and doping profile of a halo-implanted device. b) Device in a) with an LDD region added.

2b) Ion Implantation

Ion implantation is the primary method that was used to introduce halo dopants into the MOSFET. In this method, a beam of energetic ions is accelerated under high voltage and introduced into the silicon substrate where they undergo many interactions with the atoms in the lattice and electrons in the crystal. Each interaction dissipates the kinetic energy of the electron and eventually it comes to rest. Since it is a statistical process, the final distribution of implanted impurities follows a Gaussian profile which is characterized by a projected range (R_p) and a straggle (ΔR_p). [4]

For this study we used Indium implants with 60 KeV energy and a dose of 2 x 10^13 /cm^3 [5]

For this study we have used the projected range (R_p) as 27.5 nm and a straggle (ΔR_p) as 8.914 nm to calculate the junction depth of our implant which is given by the formula [4]

$$X_j = R_p \pm \Delta R_p \sqrt{2 \ln\left(\frac{N_p}{N_b}\right)} \qquad (1)$$

where X_j is the junction depth, R_p is projected range, ΔR_p is straggle of projected range, N_p is peak doping and N_b is background doping. The peak doping on the implant was assumed to be 1 x 10^{19} /cm^3. Additionally, we used doping values from previous works of Saha and his co-workers where he had the background doping as 5 x 10^{18} /cm^3 for a 20 μm channel length which was the adjusted value using Constant Field Scaling.[1]

2c) Lightly Doped Drain (LDD)

As MOSFETs become smaller, the electric field near the drain junction becomes increasingly large which can result in short channel effects such as hot-electron and punch through effects. These problems arise due to the difference in the doping between a heavily doped n+ drain region in contact with the channel. The LDD structure addresses this issue by introducing a thin, lightly doped n- region between the channel and the drain extension which reduces the electric field in the space charge region and is hence able to minimize breakdown and hot-electron effects [1]. For the device simulated in this paper, the LDD region's junction depth is one-fourth the size of the drain extension and the doping is two-thirds of the doping in the drain extension.

2d) Constant Field Scaling

Constant Field Scaling is a widely used principle to design devices that are miniaturized while maintaining their reliability. This is done by reducing device dimensions and operating voltages by a uniform scaling factor of k, which ensures that horizontal and vertical electric fields remain constant. Typically, k ≈ 0.7 is used for every generation of MOSFETs.

This study was conducted using a standard n-MOSFET provided by COMSOL Multiphysics which was then scaled down appropriately to obtain four devices of gate lengths 397 nm, 280 nm, 196 nm, and 140 nm which are 0.7 times apart. To reflect realistic behavior, the background doping concentrations were adjusted using Constant Field Scaling in accordance with the values provided in Saha et al. [3]. This allowed us to have an easier framework to directly compare devices with halo implants and conventional MOSFETs across multiple generations.

3. Governing Equations / Numerical Models

The semiconductor device simulation is based on solving a coupled system of partial differential equations, most importantly the Poisson and Continuity equations. They are then supplemented with other equations for appropriate mobility and recombination models.
The electrostatic potential V is obtained by solving the Poisson equation which in compact vector notation is written as

$$\nabla \cdot (-\epsilon_0 \epsilon_r \nabla V) = q(p - n + N_d^+ - N_a^-) \qquad (2)$$

where ϵ_0 is the permittivity of free space, ϵ_r is the relative dielectric constant, q is elementary electron charge, p is hole concentration and n is electron concentration and N_d^+ and N_a^- are the densities of ionized donors and acceptor ions.

Continuity equations that describe the conservation

of electric charge for electron and holes is given by the equations

$$\frac{\delta n}{\delta t} = \frac{1}{q}\nabla \cdot \boldsymbol{J}_n - U_n$$
$$\frac{\delta p}{\delta t} = -\frac{1}{q}\nabla \cdot \boldsymbol{J}_p - U_p \quad (3)$$

However for steady state equations, the carrier concentrations do not change over time. Assuming equilibrium, these equations can be simplified as

$$\nabla \cdot \boldsymbol{J}_p = 0\,, \quad \nabla \cdot \boldsymbol{J}_n = 0 \quad (4)$$

where $\boldsymbol{J}_n$ and $\boldsymbol{J}_p$ are electron and hole current densities and U_n and U_p are the net recombination rates. [6]
The electron and hole current densities are expressed by the following equations:

$$\boldsymbol{J_n} = qn\mu_n\nabla E_c + qD_n\nabla_n - qnD_n\nabla\ln(N_c) + qnD_{n,th}\nabla\ln(T)$$
$$\boldsymbol{J_p} = qp\mu_p\nabla E_v - qD_p\nabla_p + qpD_p\nabla\ln(N_v) + qpD_{p,th}\nabla\ln(T) \quad (5)$$

where D_n and D_p are diffusion coefficients for electrons and holes respectively and are expressed by the following equation:

$$D_n = \mu_n k_B T G\left(\frac{n}{N_c}\right)$$
$$D_p = \mu_p k_B T G\left(\frac{p}{N_v}\right) \quad (6)$$

where k_B is the Boltzmann constant, μ_p and μ_n are hole and electron mobilities, $D_{p,th}$ and $D_{n,th}$ are the hole and electron thermal diffusion coefficients and N_c and N_v are the effective density of states in the conduction and valence band.

Carrier mobilities in semiconductors can be influenced by scattering from phonons, surface roughness and high electric fields. To capture these effects, mobility models can be included in the simulation where each model can correct a specific mechanism. The models used for this simulation are the Arora Model (LI) which provides the baseline by including phonon and ionized impurity scattering, the Lombardi Model (S) which accounts for surface scattering and the Caughey-Thomas Model (E) which introduces high field velocity scattering to the model. These models can be combined in a specific hierarchy given below :

$$\mu_{total} = \mu_E(\mu_S(\mu_{LI})) \quad (7)$$

4. Experimental Results / Discussion

4a) Increase in Threshold Voltage

Threshold voltage is the applied gate voltage that is needed to achieve the threshold inversion point.[1] For the graph in Fig 2 a common way to determine threshold voltage with I_d-V_g plot is that V_T is the x-intercept of the tangent to the I_d-V_g curve taken at low V_{ds}. This method is also called linear extrapolation.
The graph in Figure 2. clearly shows us that the devices with halo implants have a higher threshold voltage than conventional MOSFETs of the same channel length.

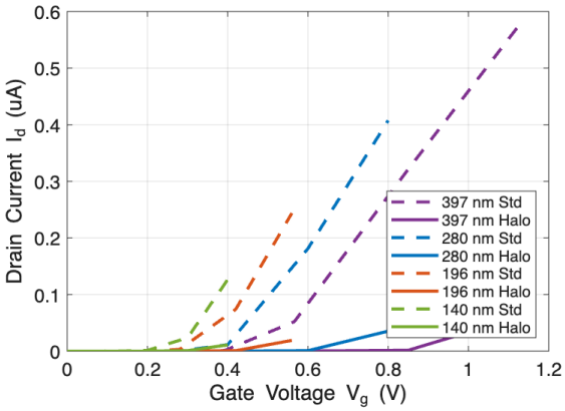


Figure 2. Id-Vg for Halo vs Standard MOSFETs for different Gate Lengths.

A halo implant typically raises the local channel doping N_A near the source and drain extensions. Mathematically, threshold voltage of a MOSFET can be given by the expression [1]

$$V_T = \frac{|Q'_{SD}(\max)|}{C_{ox}} + V_{FB} + 2\varphi_{fb} \quad (8)$$

where both $Q'_{SD}(\max)$ and $2\varphi_{fb}$ depend on N_A. When N_A increases due to Halo implants, both these terms increase and thus threshold voltage increases.

Figure 3 includes a visual representation of the device simulated in COMSOL. The device shown is a 600 nm long device (gate length 280nm) with both Halo implants and an LDD region along the channel. This schematic is representative of the structures that were simulated to generate I_d-V_g plots. The bright red indicates the source and the drain, the yellow indicates the LDD extensions whereas the two halo implants can be seen as s darker shade of blue near the terminals.

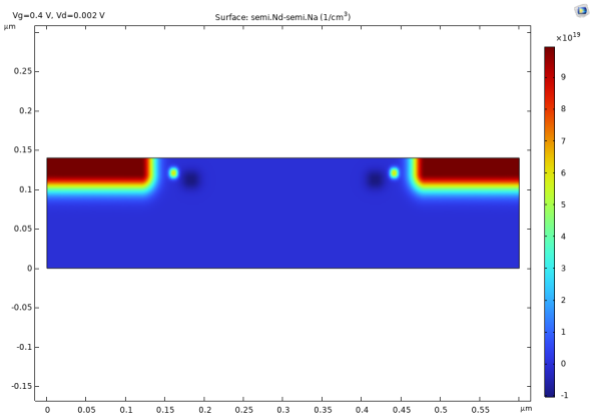


Figure 3. Schematic of n-MOSFET with halo implants and LDD extensions

4b) Decrease in Subthreshold current

The drain current that exists below the threshold voltage is called subthreshold current.[1] Below the threshold voltage, the MOSFET operates in weak inversion and the carriers cross the barrier mainly by diffusion which results in a small drain current.[2]

Figure 4 and Figure 5 compare the subthreshold current between conventional MOSFETs and MOSFETs with Halo implants. Figure 5 includes an LDD extension in both conventional and halo implanted MOSFETs to further analyze the trends. For both cases (with and without LDD extension) we can notice a sharp decrease in the subthreshold current for the Halo implanted MOSFETs. These observations align with previous work done by Hueting and his coworkers who show that the off current is mostly governed by the subthreshold current which is largely determined by the 2-D hole distribution in the channel which can be controlled by introducing Halo implants.[2]

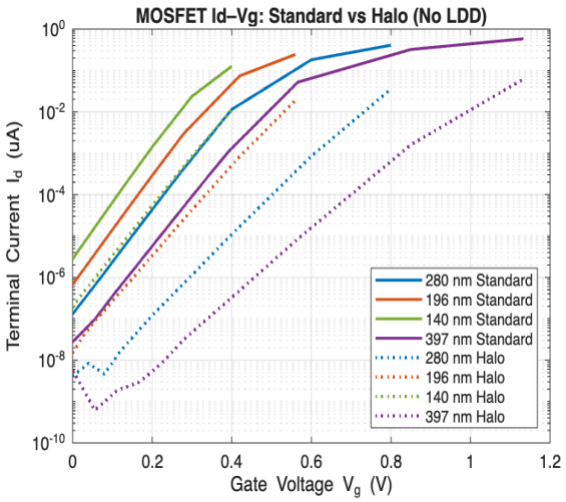


Figure 4. Id-Vg plots for Halo vs Std MOSFET without LDD region

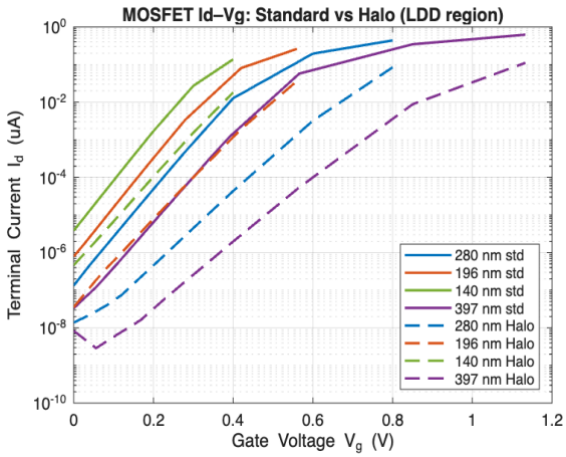


Figure 5. Id-Vg plots for Halo vs Std MOSFET with LDD region

Conclusion

The incorporation of halo implants in MOSFET devices demonstrated a significant improvement in threshold voltage roll-off and a reduction in subthreshold current. These enhancements suggest that halo doping can effectively mitigate short-channel effects and improve overall device performance. Future work can be focused on refining the mesh further to get more precise results especially in the regions with increased activity. We could also incorporate more physics and different mobility models that could play a role in providing more precise results. A further quantitative analysis of the data could also be very helpful in understanding subthreshold behaviour.

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